REMARKS

The Office Action of November 19, 2005, has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested.

Claims 47-60, 62, 63, and 65-66 are pending. No claims have been amended. The above listing of claims is presented for the Examiner's convenience.

Rejection of Claims Over Hemink

Claims 47-60, 62, 63, and 65-66 stand rejected under 35 U.S.C. § 102(a) over Hemink. Applicants traverse.

Claim 47 recites, *inter alia*:

> " a first bit line connected to said first memory cell section;
>
> a second bit line connected to said second memory cell section, being different from said first bit line; ...
>
> wherein first program /read data of said first memory cell is latched in said latch circuit, while second program /read data of said second memory cell is held by said second bit line."

Support for this claim may be found at least in Figures 60A-60D.

In contrast, according to Hemink et al., the first and second signal lines, which the Examiner indicated, are in fact the same line. They are electrically shorted together. Because they are shorted together, they cannot be the first and second bit lines, respectively. The Examiner has listed one element of Hemink and asserted that it relates to two elements in Applicants' claims. This is incorrect. See Figure 13 of Hemink. Hemink does not disclose the latch connected to two bit lines. With this structure, Hemink et al. cannot realize the action that data of a first memory cell is latched in a latch circuit while data of a second memory cell is held by the second signal line as claimed.

Hemink does not disclose the operation of the first and second bit lines as claimed. The structure of Figure 13 does not disclose "first program /read data of said first memory cell is latched in said latch circuit, while second program /read data of said second memory cell is held by said second bit line."

The other independent claims and dependent claims are allowable for similar reasons.

Rejection of Claims Over Sakui

Claims 47-60, 62, 63, and 65-66 stand rejected under 35 USC 102(e) over Sakui et al. Applicants traverse.

Claim 47 recites, *inter alia*:

> " a first bit line connected to said first memory cell section;
>
> a second bit line connected to said second memory cell section, being different from said first bit line; ...
>
> wherein first program /read data of said first memory cell is latched in said latch circuit, while second program /read data of said second memory cell is held by said second bit line."

Support for this claim may be found at least in Figures 60A-60D.

The Examiner has cited Figure 38 against the present claims. Figure 38 of Sakui et al. does not relate to the recitations of claim 47. Column 33, lines 27-39 of Sakui et al. indicate that the data circuit of Figure 38 relates to storing data in pairs.

> " FIG. 38 shows an arrangement using a differential sense amplifier. In this case, 1-bit data may be stored in two memory cell units as complementary data. Data is read by detecting a small difference between signal amounts (potentials) output from the two memory cell units and amplifying this difference. This allows a high-speed read.
>
> One-bit data is stored in a pair of memory cell units. For this reason, even when the program/erase endurance characteristics of one memory cell unit degrade due to the repeated data change operation, the reliability does not decrease as far as the other memory cell unit has satisfactory program/erase endurance characteristics."

Both the left and right side memory cells are accessed in parallel using BLi and /BLi. In other words, they operate the same way at the same time. This is different from the recitations of claim 47.

In FIG. 38 of Sakui et al., a first bit line BLi is connected to a node of a latch circuit, which is different from a node of the latch circuit, a second bit line /BLi is connected to. In other words, as in FIGS. 13 and 20 of Hemnik et al., the first and second bit lines are not connected to a common node of the latch circuit. In addition, Sakui et al. does not disclose that data of a first memory cell is latched in the latch circuit while data of a second memory cell is held in the second bit line. Therefore, the present invention is not anticipated by Sakui et al.

The other independent claims and dependent claims are allowable for similar reasons.

It is believed that no fee in addition to the extension of time fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733 accordingly. No additional claim fees are believed due. If any fees are due, the Commissioner is authorized to debit our deposit account no. 19-0733.

Respectfully Submitted,

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